## REMARKS

Reconsideration of the above-identified application in view of the foregoing amendments and following remarks is respectfully requested.

A. Claim Status / Explanation of Amendments

Claims 1-20 are pending and were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 6,972,635 to McCorquodale, et al. ("McCorquodale") in view of U.S. Patent No. 6,362,698 to Gupta ("Gupta") and further in view of U.S. Patent No. 6,268,778 to Mucke, et al. ("Mucke") and publication IEEE, ISSCC Vol. 12/2001 to Weldon, et al. ("Weldon"). [10/9/07 Office Action, p. 2].

By this paper, claims 1 and 2 are amended. Claim 1 is amended to recite, *inter alia*, a "PLL synthesizer having a programmable counter, ... wherein the programmable counter divides an output signal of the voltage controlled oscillator." Claim 2 is amended to recite, *inter alia*, a "second frequency divider circuit provided separately from the PLL synthesizer." Both claim 1 and 2 are amended to include the limitation wherein a "frequency of the voltage controlled oscillator is controlled to be a frequency n times a target frequency so that it is possible to form the inductor and the capacitor of the voltage controlled oscillator on a semiconductor IC, a division ratio of the frequencyircuit is set to be 1/n so that a frequency of the output signal of the voltage controlled oscillator is made to be 1/n." Support for the amendments to claims 1 and 2 may be found throughout the application as originally filed including, for example, p. 2, ln. 22 to p. 3, ln. 10 and p. 10, lns. 21-23.

No new matter will be introduced into this application by entry of these amendments. Entry is respectfully requested.

B. Claims 1-20 are Patentably Distinct from the Cited References

Applicants respectfully traverse the 35 U.S.C. § 103(a) rejection of claims 1-20 over McCorquodale in view of Gupta and further in view of Mucke and Weldon. As set forth in detail below, the cited references, whether taken singly or in combination, do not teach, disclose or suggest each and every element of Applicants' independent claims 1 and 2. Accordingly, a rejection for obviousness is improper.

Applicants' claim 1, as amended, recites:

> 1. An oscillator circuit, comprising:
>
> a voltage controlled oscillator having an inductor and a variable capacitor configured to generate an output signal having a frequency of n times of a target frequency;
>
> a PLL synthesizer having a programmable counter, a phase detector and a control voltage generation circuit, wherein the programmable counter divides an output signal of the voltage controlled oscillator, the phase detector is configured to detect phase difference between the output signal from the programmable counter and a reference signal, and the control voltage generator circuit is configured to generate a control signal of the voltage controlled oscillator based on the phase information detected at the phase detector so that the voltage controlled oscillator is controlled to generate the output signal having a frequency of n times of the target frequency,
>
> a frequency divider circuit provided separately from the PLL synthesizer, dividing the output signal from the voltage controlled oscillator into 1/n frequency and generating at least two signals having an equal frequency and different phases by 180° from each other,
>
> wherein a frequency of the voltage controlled oscillator is controlled to be a frequency n times a target frequency so that it is possible to form the inductor and the capacitor of the voltage controlled oscillator on a semiconductor IC, a division ratio of the frequency divider circuit is set to be 1/n so that a frequency of the output signal of the voltage controlled oscillator is made to be 1/n, and the voltage controlled oscillator, the PLL synthesizer, and the frequency divider circuit are formed on a semiconductor integrated circuit.

McCorquodale is directed to MEMS-based computer systems, clock generation and oscillator circuits, and an LC-tank apparatus for use therein. [McCorquodale, Abstract]. .In one embodiment, as shown by Fig. 8b below, McCorquodale discloses that a:

> ... clock oscillator provides a differential output signal that drives a single-ended to differential converting amplifier with unity gain. A series of flip-flops then divide the signal to the appropriate frequency. [McCorquodale, Col. 22, lns. 1-6].

The Office Action contends that McCorquodale's series of flip-flops which divide the signal output from the voltage controlled oscillator (VCO) corresponds to Applicants' "frequency divider circuit ... dividing the output signal from the voltage controlled oscillator into 1/n frequency" as recited in pending claim 1. [10/9/07 Office Action, p. 3]. However, the frequency of Applicant's VCO and division ratio of Applicants' frequency divider circuit are interrelated. That is, when the output signal from the VCO is set to a frequency of n times a target frequency, the frequency divider circuit also factors the output signal by 1/n.

McCorquodale, on the other hand, does not set the division ratio of the flip-flops in Fig. 8b at a plurality of steps as 1/n such that an oscillation frequency having been set to be n times a target frequency is made to be 1/n. This patentable distinction is recited in Applicants' claim 1 as the limitation wherein a "division ratio of the frequency divider circuit is set to be 1/n so that a frequency of the output signal of the voltage controlled oscillator is made to be 1/n." Applicants respectfully assert that McCorquodale fails to teach, disclose, or suggest this

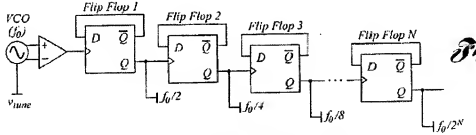


Fig. 8b

[McCorquodale, Fig. 8b].

relationship between the VCO and frequency divider circuit. Furthermore, the deficiency in McCorquodale cannot be remedied by the introduction of Gupta, Mucke, or Weldon which are cited as disclosing a PLL system, a MOSFET as an integrated capacitor, and a mixer, respectively. [10/9/07 Office Action, p. 3-4]. Applicants' own review reveals that none of the cited references disclose the relationship between the division ratio of the frequency divider circuit and the frequency of the output signal of the VCO as discussed above.

Accordingly, McCorquodale, Gupta, Mucke, and Weldon – whether alone or in combination – fail to teach, disclose, or suggest an oscillator circuit wherein "a frequency of the voltage controlled oscillator is controlled to be a frequency n times a target frequency so that it is possible to form the inductor and the capacitor of the voltage controlled oscillator on a semiconductor IC, a division ratio of the frequency divider circuit is set to be 1/n so that a frequency of the output signal of the voltage controlled oscillator is made to be 1/n" as recited in Applicants' amended claim 1. Applicants submit claim 1 is patentably distinct from the cited references for at least this reason. Since claim 2 is directed to an oscillator circuit reciting the above limitation it is also asserted to be in condition for allowance. Dependent claims 3-20 are also believed to define patentable subject matter for at least similar reasons.

Applicants have chosen in the interest of expediting prosecution of this patent application to distinguish the cited documents from the pending claims as set forth above. These statements should not be regarded in any way as admissions that the cited documents are, in fact, prior art. Likewise, Applicants have chosen not to swear behind the references cited by the Office Action, or to otherwise submit evidence to traverse the rejection at this time. Applicants, however, reserve the right, as provided by 37 C.F.R. §§ 1.131 and 1.132, to do so in the future as appropriate. Furthermore, Applicants have not specifically addressed the rejections of the

dependent claims. Applicants respectfully submit that the independent claims, from which they depend, are in condition for allowance as set forth above. Accordingly, the dependent claims also are in condition for allowance. Applicants, however, reserve the right to address such rejections of the dependent claims in the future as appropriate.

## CONCLUSION

For the above-stated reasons, this application is respectfully asserted to be in condition for allowance. An early and favorable examination on the merits is earnestly solicited. In the event that a telephone conference would facilitate the examination of this application in any way, the Examiner is invited to contact the undersigned at the number provided.

THE COMMISSIONER IS HEREBY AUTHORIZED TO CHARGE ANY ADDITIONAL FEES WHICH MAY BE REQUIRED FOR THE TIMELY CONSIDERATION OF THIS AMENDMENT UNDER 37 C.F.R. §§ 1.16 AND 1.17, OR CREDIT ANY OVERPAYMENT TO DEPOSIT ACCOUNT NO. 13-4500, ORDER NO. 5000-5247.

Respectfully submitted,
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